Reconfiguring Capacitors in Rechargeable Power Sources for Longer Sustainable Power

SuperCaps are replacing rechargeable batteries in stored power applications. The capacitors are usually connected in series for rapid charging using a set of switches and reconfigured into parallel for sourcing power. On the load side, Electronic loads (devices) may have a voltage threshold limitation below the threshold voltage they may not draw current leaving substantial residual charge on the source capacitors.

Intuitively, the source capacitors charged to the threshold voltage when reconnected in series could supply additional power until the overall voltage drops to the threshold level. However, the aggregate capacitance in series topology reduces to its lowest value and the charge depletes quickly. It is interesting to note that connecting capacitors in mixed series-parallel combinations yield better results.

The work reported here investigates two aspects: i) compare various combinations in which source capacitors charged to threshold voltage may be reconfigured to prolong the power source life. ii) Switching hardware complications that arise in implementing those configurations.

Case I:

In this case study the rechargeable source comprises of 4 capacitors, 1F each for simplicity and charged to 3.6V arbitrarily by external means. The capacitors connected in parallel drive the load as shown in Fig: 1(a). The load draws 300mA for inputs above 1.8V threshold while no current flows below the threshold, leaving a corresponding residual charge Q = C*V or 4F*1.8V = 7.2 Coulomb, on the source capacitors.

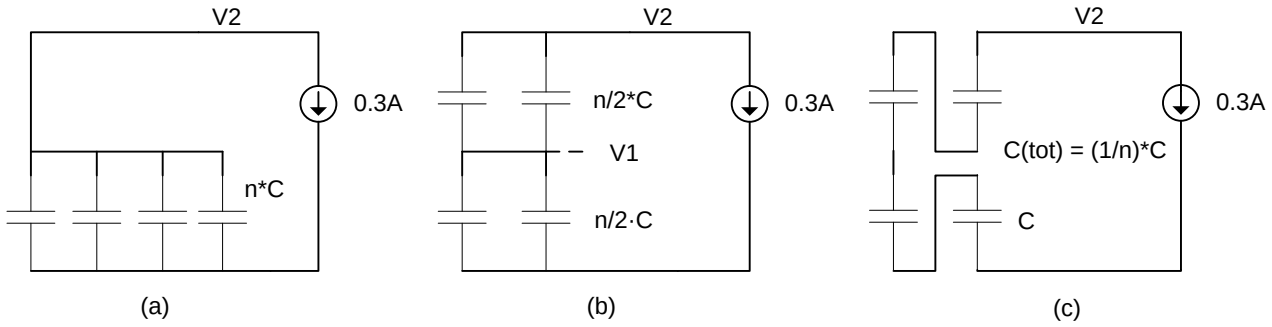


Fig: 1 A bank of 4-Supercaps for this discussion.

Based on a simple algorithm, the parallel bank of charged capacitors is split evenly, two capacitors each for this example, both at 1.8V. The half-banks are stacked as in Fig: 1(b), doubling the overall voltage back to 3.6V. The capacitors are drained again at a constant rate of 300mA until the overall voltage drops to 1.8V. The process is repeated with the half-banks split into quarter-banks (1/4 of total), then for larger number of capacitors those stacks split again and so on. In this 4 capacitors example the last split arrives quickly for the final configuration of all capacitors in series, Fig: 1(C). At the end of the last cycle each capacitor is left with 1.8V/4 or 0.45V.

Starting with a large number of capacitors, one could go on reconfiguring the capacitors and reducing the residual charge however, the advantage diminishes quickly in view of the exponential growth of hardware.

AgileAccess™, LLC
23 Londonderry Drive, Flemington, NJ 08822 **USA**
Ph: 1+ (908) 788-7740 ● e-mail: contact@agileaccess.com

1) All capacitors in parallel as in Fig: 1(a), the useful life of the bank of 4 capacitors (each 1F for computational convenience), charged to 3.6V, is simply Q = CV, next dQ/dt = i, so C*V = i*time :

(3.6V - 1.8V)*4F/0.3A = t (1)

t = 24 sec

2) Second iteration: a stack of two high, two-parallel capacitors each in Fig: 1(b) above:
The time it takes for the stack of n = 2 caps each 1F, to discharge down to 1.8V:

(3.6V – 1.8V) x [Ceq] = 0.3A x t --how much time ?

Ceq = [1/(C1+C2) + 1/(C3+C4)]^-1 ; Ceq = 1F --each cap being 1F.

t = [1.8V x 1F]/0.3A

t = 6 sec

The 6 sec time may be added to the power source life (24 sec) by an automated switching arrangement, for a 25% improvement. Note that each capacitor at the end of second cycle carries 0.9V across it, and may now be reconnected in series producing 3.6V again, for another go around.

V2 = 1.8V V1 = 0.9V (V2 – V1) = 0.9V

3) Upon the final series configuration, and draining the charge:

(3.6V – 1.8V) x [Ceq] = 0.3A x t

1/Ceq = [1/C + 1/C + 1/C +1/C) ; Ceq = (1/4)F

t = [1.8V x 0.25F]/0.3A

t = 1.5 sec

The total time gained is 7.5 sec, or 31% more life, however, at the expense of switching the capacitors around and losing some time in the switching transients. This last step may call for cost benefit evaluation.

For reference, if all capacitors had been placed in series directly, bypassing Fig: 1(b) the gain would be:

(4*1.8V – 1.8V) x [Ceq] = 0.3A x t

1/Ceq = [1/C + 1/C + 1/C +1/C) ; Ceq = (1/4)F

t = [5.4V x 0.25F]/0.3A

t = 4.5 sec

The improvement is 18.75% only, while step 2, a solid 25%, besides 31% additional switching permitted.

Switch Matrix:

Fig: 2 -4 show a modular scalable switch matrix which can deliver the above described 'half-stack' configurations and a few more. The needed control for the switches is included in the control table.

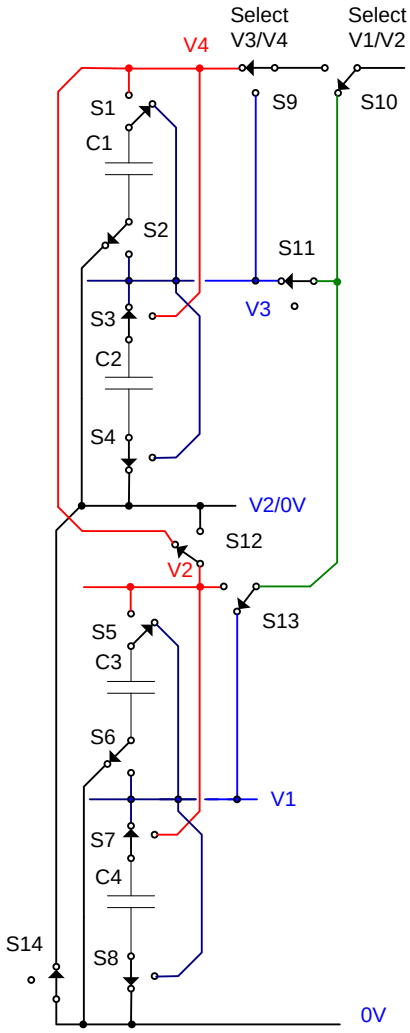


Fig: 2 All Caps in parallel

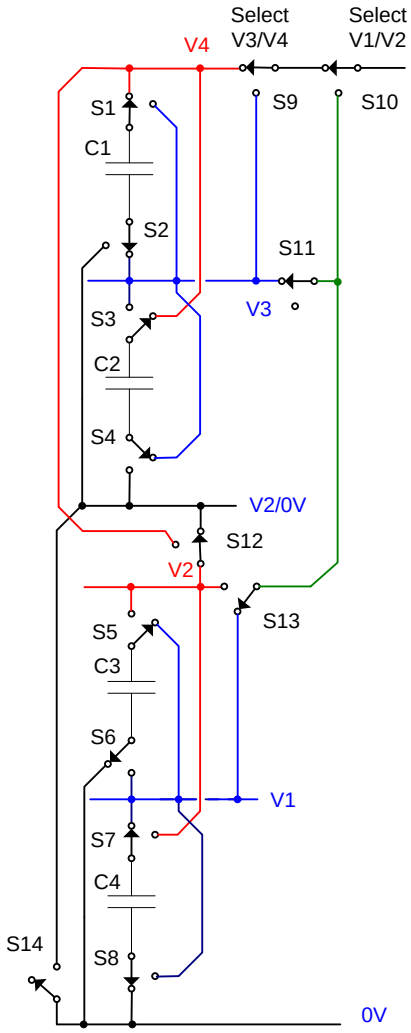


Fig: 3 Half-Stacks

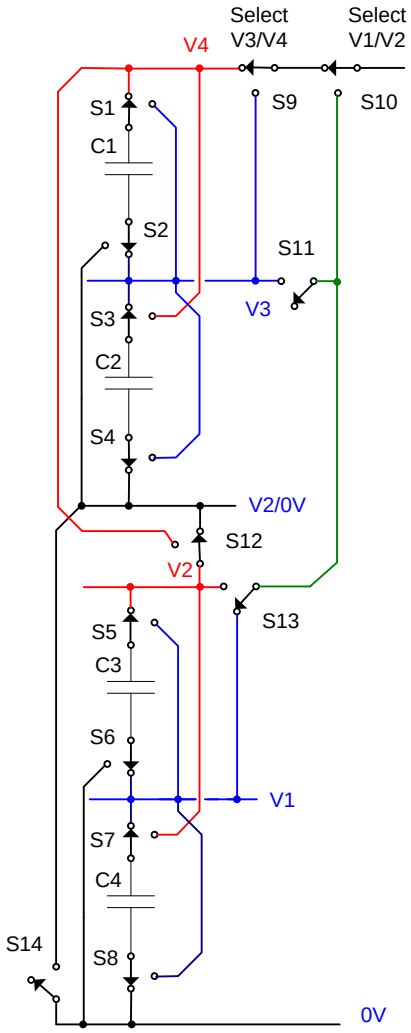
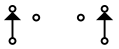
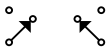


Fig: 4 All in series

Note that the matrix includes additional switches for convenience, and may be removed as shown below.

Control Table:

X =  O =  - = Don't Care

No:	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	Comments
A	o	o	x	x	o	o	x	x	x	o	x	o	o	x	Fig:2 All parallel
Y	x	x	o	o	o	o	x	x	x	x	x	-	o	o	Fig:3 Half-Stacks
Z	x	x	x	x	x	x	x	x	x	x	o	x	x	o	Fig:4 All series

AgileAccess™, LLC
23 Londonderry Drive, Flemington, NJ 08822 **USA**
Ph: 1+ (908) 788-7740 ● e-mail: contact@agileaccess.com

The switch matrix design is a topic in itself and dealt with elsewhere. The number of switches required for implementing 'all capacitors in series' for charging, and 'all capacitors in parallel' for delivering power, is roughly 2(n-1) where 'n' is the number of capacitors to be switched. The remaining configurations may take additional switches. For the first cut switches may be inserted judiciously to meet the configuration requirements and later the design optimized by removing redundant switches as described below.

In the above table if A, Y, and Z states corresponding to parallel, half-stacks and all series capacitor configurations; were the only states to be realized then several of the switches that do not change state between the rows may become redundant. For example S7, S8, S9 may be replaced by shorts while some of the remaining eg: S10-14 may be simplified (opened) if there are any hidden 'don't care' states among them.

While programming the control of switches care should be taken in opening or closing the switches, making sure that the capacitors are not getting momentarily shorted while reconfiguring, or inadvertently placed in circuit when they should be isolated to preserve charge. This requirement takes additional switches to implement.

Observations:

The total capacitance needed to store the required energy and its distribution over number of capacitors is a design parameter for consideration. On one hand more capacitance is needed for more energy and longer sustainability, and more capacitors also help in lowering residual charge by building higher stacks. However, more capacitors add to the overall volume, and are difficult to charge in tall stacks, besides requiring more switches to meet additional configuration demands.

It is interesting to note that stacking the capacitors in other configurations may hold advantage over the symmetric split of Case-I. For example forming uneven stacks, one capacitor on top of three capacitors in parallel and discharging those to 1.8V. The single capacitor is then replaced by another from the parallel bank below while holding the discarded one in isolation and so on. This scheme of 'one capacitor at a time' is explored in Case-II.

Case II:

Splitting capacitors in un-even parallel banks and stacking them, with fewer capacitors stacked on top of a larger bank of parallel caps, whether there is an advantage over Case-I scheme.

The 4 capacitor example is picked again for comparison, this time with a different stacking order in Fig: 5.

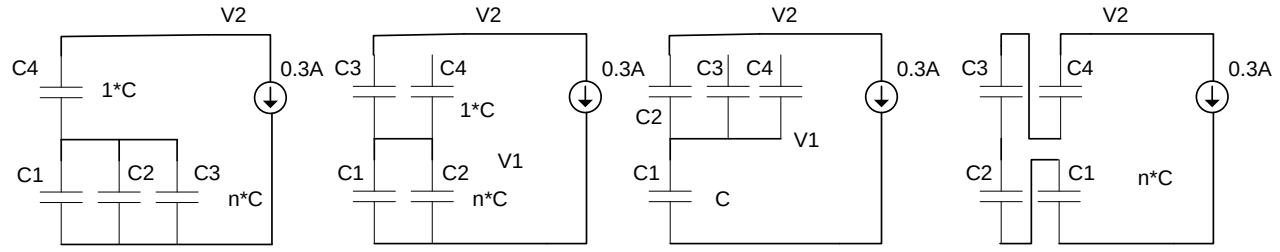


Fig: 5 One capacitor at a time.

1) Starting with the time it takes for the stack of one cap over 3 caps in parallel, discharge down to 1.8V:

(3.6V – 1.8V) x [Ceq] = 0.3A x Time (t) --how much time ? Where

Ceq = [1/(C1+C2+C3) + 1/ C4]^-1 ; Ceq = 3/4F --each cap being 1F.

t = [1.8V x 3/4*F]/0.3A

t = 4.5 sec

2) Next the capacitor C4 is isolated and replaced by C3 from the parallel bank; which is now at a different voltage than the previous case.

V2 = 1.8V V1 = 1.35V while C4 voltage = V2 - V1 = 0.45V

(2.7V – 1.8V) x [Ceq] = 0.3A x Time (t)

Ceq = [1/(C1+C2)+1/C3)]^-1 = 2/3 F --each cap being 1F.

t = [0.9V x 2/3*F]/0.3A

t = 2 sec

3) Moving to the next configuration only two capacitors C1 and C2 in series with new voltages:

V2 = 1.8V V1 = 1.2V while C3 voltage = 0.6V

(2.4V – 1.8V) x [Ceq] = 0.3A x Time (t)

Ceq = [1/C1+1/C2]^-1 = 1/2 F

t = [0.6V x 1/2*F]/0.3A

t = 1 sec

4) The last configuration where all capacitors at various voltages from above, are placed in series:

C4 @ 0.45V C3 @ 0.6V C2 = C1 = 0.9V

(2.85V – 1.8V) x [Ceq] = 0.3A x Time (t)

Ceq = [1/C1+1/C2+1/C3+1/C4]^-1 = 1/4 F

t = [1.05V x 1/4*F]/0.3A 3.5/4 = 0.875 sec

t = 0.875 sec

The total time for this scheme: t = 4.5 + 2 + 1 + 0.875 sec = 8.375 sec

The advantage over the two-step symmetric split method: t = 7.5 sec is about 0.875 sec or 11.7% better, and overall improvement at 35% compared with 31% for the symmetric method, with more switching time of course. However, as seen below this advantage comes at the cost of complex switch matrix.

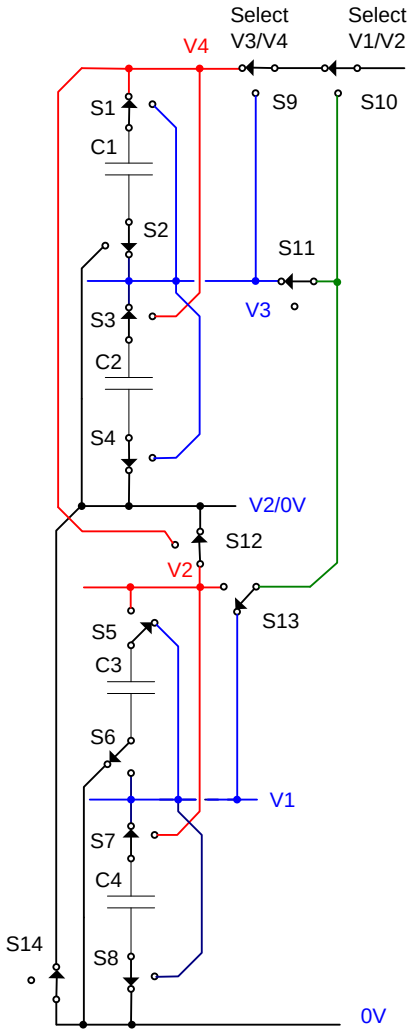


Fig: 6 C1 on C2//C3//C4

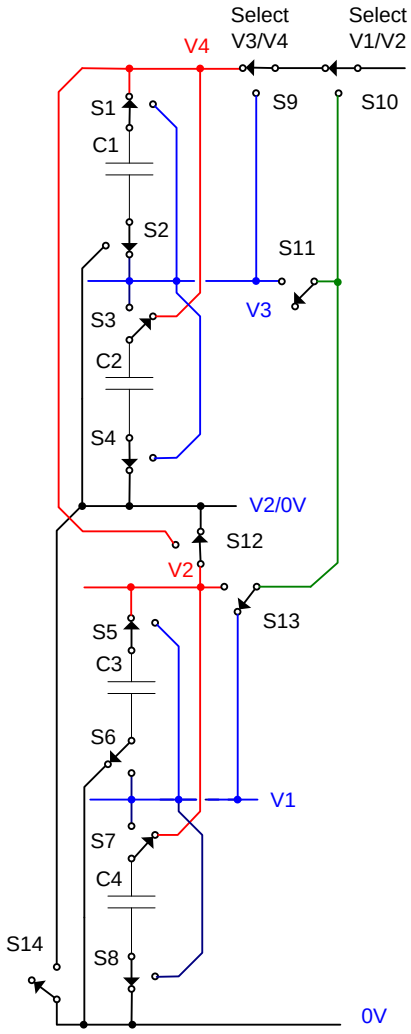


Fig: 7, C2 on C3//C4

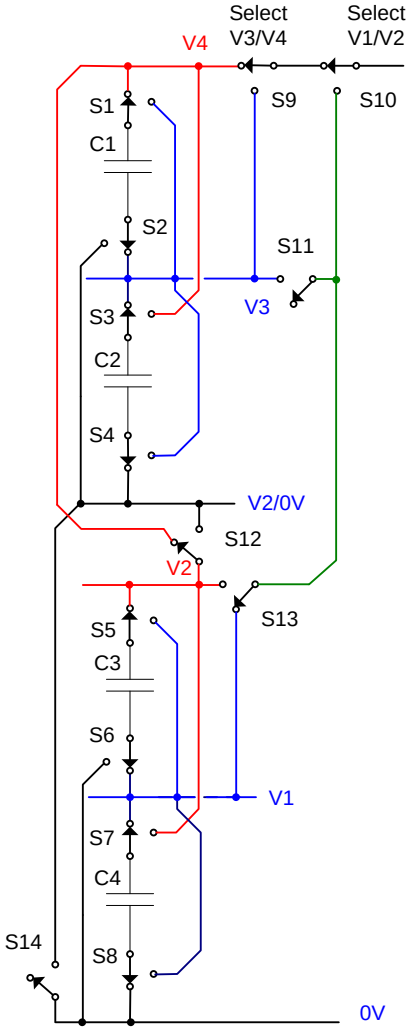
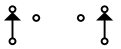
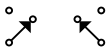


Fig: 8, C3, C4 in series

Control Table:

X =  O =  - = Don't Care

No:	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	Comments
A	o	o	x	x	o	o	x	x	x	o	x	o	o	x	All parallel
B	x	x	x	x	o	o	x	x	x	x	x	-	o	x	Fig:2 C4 on C1,C2,C3
C	x	x	o	x	x	o	o	x	x	x	o	x	o	o	Fig:3 C3 on C1,C2
D	x	x	x	x	x	x	x	x	x	x	o	o	-	o	Fig:4 C1,C2 only
Z	x	x	x	x	x	x	x	x	x	x	o	x	x	o	All series

Case II uses all five states starting with A, All Parallel and ending in Z, All Series. The A and Z states are shown in Case I. Between states A thru Z several of the switches that do not change state between the rows, may become redundant. For this example S4, S8, and S9 may be eliminated by shorting.

Observations:

Uneven stacks achieve higher effective capacitance compared with the all in series configuration, as a result more sustainability, however, at the cost of more switches and configurations.

The switch matrix design used in the above examples could have been simpler using fewer switches. For the sake of convenience, a common single design as it appears in Fig: 3-4 and Fig: 6-8 was chosen. The main challenge in Case-II switch matrix architecture remains in providing means (switches) for isolating the capacitor(s) which have been partially depleted of the residual charge, and have a lower voltage across. Intuitive matrix architectures do not support this feature and inevitably return each capacitor back to the circuit where it may exchange charge with other capacitors (supplying or receiving) and perhaps lose the above cited narrow advantage.

Note: The above examples have not been verified by prototype at the posting of this article. Prototyping along with switch control electronics may be carried out later and results shared as they become available. Please feel free to forward your comments to the contact below.